



PTH12010 12Vin Single

Application Note 160

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1. Introduction

The PTH family of non-isolated, wide-output adjust power modules from Artesyn Technologies are optimized for applications that require a flexible, high performance module that is small in size. These products are part of the “Point-of-Load Alliance” (POLA), which ensures compatible footprint, interoperability and true second sourcing for customer design flexibility. The POLA is a collaboration between Artesyn Technologies, Astec Power, Texas Instruments and Ericsson Power Modules to offer customers advanced non-isolated modules that provide the same functionality and form factor. Product series covered by the alliance includes the PTHxx050 (6 A), PTHxx060 (10 A), PTHxx010 (15/12 A), PTHxx020 (22/18 A), and the PTHxx030 (30/26 A).


From the basic, “Just Plug it In” functionality of the 6 A modules, to the 30 A rated feature-rich PTHxx030, series these products were designed to be very flexible, yet simple to use. The features vary with each product series. Table 1 provides a quick reference to the available features by series and input bus voltage.

For simple point-of-use applications, the PTHxx050 series provides operating features such as an on/off inhibit, output voltage trim, pre-bias start-up (3.3/5 V input only), and overcurrent protection. The PTHxx060 (10 A), and PTHxx010 (15/12 A) series add an output voltage sense, and margin up/down controls. The higher output current, PTHxx020 and PTHxx030 series also incorporates overtemperature and shutdown protection. All of the products referenced in Table 1 include Auto-Track™.

This is a feature unique to the PTH family, and was specifically designed to simplify the task of sequencing the supply voltage in a power system. These and other features are described in the following sections.

SERIES	INPUT BUS	I _{OUT}	ADJUST TRIM	ON/OFF INHIBIT	OVER-CURRENT	PREP-BIAS START-UP	*AUTO-TRACK™	MARGIN UP/DOWN	OUTPUT SENSE	THERMAL SHUTDOWN
PTHxx050	3.3 V	6 A	●	●	●	●	●			
	5 V	6 A	●	●	●	●	●			
	12 V	6 A	●	●	●	●	●			
PTHxx060	3.3/5 V	10 A	●	●	●	●	●	●	●	
	12 V	10 A	●	●	●	●	●	●	●	
PTHxx010	3.3/5 V	15 A	●	●	●	●	●	●	●	
	12 V	12 A	●	●	●	●	●	●	●	
PTHxx020	3.3/5 V	22 A	●	●	●	●	●	●	●	●
	12 V	18 A	●	●	●	●	●	●	●	●
PTHxx030	3.3/5 V	30 A	●	●	●	●	●	●	●	●
	12 V	26 A	●	●	●	●	●	●	●	●

Table 1 - Operating Features by Series and Input Bus Voltage

RoHS Compliance Ordering Information	
	PTH12010WAST To order Pb-free (RoHS compatible) surface-mount parts replace the mounting option ‘S’ with ‘Z’, e.g. PTH12010WAZ. To order Pb-free (RoHS compatible) through-hole parts replace the mounting option ‘H’ with ‘D’, e.g. PTH12010WAD.

*Auto-track™ is a trade mark of Texas Instruments



2. System Interface Information

2.1 Input Capacitor

The recommended input capacitor(s) is determined by the 560 μF minimum capacitance and 800 mArms minimum ripple current rating. A 10 μF X5R/X7R ceramic capacitor may also be added to reduce the reflected input ripple current. The ceramic capacitor should be located between the input electrolytic and the module.

Ripple current, less than 100 m Ω equivalent series resistance (ESR) and temperature are major considerations when selecting input capacitors. Unlike polymer-tantalum capacitors, regular tantalum capacitors have a recommended minimum voltage rating of 2 x (max. dc voltage + ac ripple). This is standard practice to ensure reliability. Only a few tantalum capacitors have sufficient voltage rating to meet this requirement. At temperatures below 0 °C, the ESR of aluminum electrolytic capacitors increases. For these applications Os-Con, polymer-tantalum, and polymer-aluminum types should be considered.

2.2 Output Capacitance (Optional)

For applications with load transients (sudden changes in load current), regulator response will benefit from external output capacitance. The value of 330 μF is used to define the transient response specification (see datasheet). For most applications, a high quality computer-grade aluminum electrolytic capacitor is adequate. These capacitors provide decoupling over the frequency range, 2 to 150 kHz, and are suitable for ambient temperatures above 0 °C. Below 0 °C, tantalum, ceramic or Os-Con type capacitors are recommended. When using one or more non-ceramic capacitors, the calculated equivalent ESR should be no lower than 4 m Ω (7 m Ω using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 2.

In addition to electrolytic capacitance, adding a 10 μF X5R/X7R ceramic capacitor to the output will reduce the output ripple voltage and improve the regulator's transient response. The measurement of both the output ripple and transient response is also best achieved across a 10 μF ceramic capacitor.

2.2.1 Tantalum Capacitors

Tantalum type capacitors are most suited for use on the output bus, and are recommended for applications where the ambient operating temperature can be less than 0 °C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution many general purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable as they have no surge current rating. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications.

When specifying Os-con and polymer tantalum capacitors for the output, the minimum ESR limit will be encountered well before the maximum capacitance value is reached.

2.2.2 Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 300 μF . Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 μF or greater.

2.2.3 Capacitor Table

Table 2 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

2.2.4 Designing for Very Fast Load Transients

The transient response of the dc-dc converter has been characterized using a load transient with a di/dt of 1 A/ μs . The typical voltage deviation for this load transient is given in the datasheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc-dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

If the transient performance requirements exceed that specified in the datasheet, or the total amount of load capacitance is above 3,000 μF , the selection of output capacitors becomes more important.

CAPACITOR VENDOR/ SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR PART NUMBER
	WORKING VOLTAGE	VALUE (μ F)	MAX. ESR AT 100 kHz	MAX RIPPLE CURRENT AT 85°C (Irms)	PHYSICAL SIZE (MM) (L X W)	INPUT BUS	OPTIONAL OUTPUT BUS	
Panasonic FC (Radial) FK (SMD)	25 V 35 V 25 V	560 1000 680	0.065 Ω 0.060 Ω 0.060 Ω	1205 mA 1100 mA 1100 mA	12.5 x 15 12.5 x 13.5 12.5 x 13.5	1 1 1	1 1 1	EEUFC1E561S EEVFK1E102Q EEVFK1V681Q
United Chemi-Con FX, OS-CON (SMD) LXZ (Radial) PS (Radial) PXA (SMD)	16 V 16 V 16 V 16 V	330 330 680 330	0.018 Ω 0.014 Ω 0.068 Ω 0.014 Ω	4500 mA 5050 mA 1050 mA 5050 mA	10.0 x 10.5 10.0 x 12.5 10.0 x 16.0 10.0 x 12.2	2 2 1 2	\leq 3 \leq 2 1 \leq 2	16FX330M 16PS330MJ12 LXZ16VB681M10X16LL PXA16VC331MJ12
Nichicon PM (Radial) HD (Radial)	25 V 16 V 35 V	560 680 560	0.060 Ω 0.038 Ω 0.048 Ω	1060 mA 1430 mA 1360 mA	12.5 x 15.0 10.0 x 16.0 16.0 x 15.0	1 1 1	1 1 1	UPM1E561MHH6 UHD1C681MHR UPM1V561MHH6
Panasonic, Poly-Aluminum WA (SMD) S/SE (SMD)	16 V 6.3 V	330 180	0.022 Ω 0.005 Ω	4100 mA 4000 mA	10.0 x 10.2 7.3 x 4.3	1 N/R ⁽²⁾	\leq 3 \leq 1 ⁽¹⁾	EEFWA1C331P EEFSE0J181R ($V_o \leq 5.1$ V)
SANYO Os-Con TPE (SMD) SP (Radial) SVP (SMD)	10 V 16 V 16 V	330 270 330	0.025 Ω 0.018 Ω 0.016 Ω	>3000 mA >3500 mA >4700 mA	7.3 x 5.7 10.0 x 10.5 11.0 x 12.0	N/R ⁽²⁾ 2 ⁽¹⁾ 2	\leq 4 \leq 3 \leq 3	10TPE330M 16SP270M 16SVP330M
AVX Tantalum TPS (SMD)	10 V 10 V	470 330	0.045 Ω 0.045 Ω	>1723 mA >1723 mA	7.3 x 5.7 7.3 x 5.7	N/R ⁽²⁾ N/R ⁽²⁾	\leq 5 ⁽³⁾ \leq 5 ⁽³⁾	TPSE477M010R0045 ($V_o \leq 5.1$ V) TPSE337M010R0045 ($V_o \leq 5.1$ V)
Kemet T520 (SMD) T530 Poly-Tant/ Organic	10 V 10 V 6.3 V	330 330 470	0.040 Ω 0.015 Ω 0.012 Ω	1800 mA >3800 mA >4200 mA	4.3 x 6.0 4.3 x 6.0 4.3 x 6.0	N/R ⁽²⁾ N/R ⁽²⁾ N/R ⁽²⁾	\leq 5 \leq 2 \leq 2 ⁽³⁾	T520X337M010AS T530X337M010AS T530X477M006AS ($V_o \leq 5.1$ V)
Vishay-Sprague 595D (SMD) 94SP (Radial)	10 V 16 V	470 270	0.100 Ω 0.018 Ω	1440 mA 4200 mA	7.2 x 6.0 10.0 x 10.5	N/R ⁽²⁾ 2 ⁽¹⁾	\leq 5 ⁽³⁾ \leq 3	595D477X0010R2T ($V_o \leq 5.1$ V) 94SP277X0016FBP
Kemet, Ceramic X5R (SMD)	16 V 6.3 V	10 47	0.002 Ω 0.002 Ω		1210 case 3225mm	1 ⁽⁴⁾ N/R ⁽²⁾	\leq 5 \leq 5	C1210C106M4PAC C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3 V 6.3 V 16 V 16 V	100 47 22 10	0.002 Ω		1210 case 3225mm	N/R ⁽²⁾ N/R ⁽²⁾ 1 ⁽⁴⁾ 1 ⁽⁴⁾	\leq 3 \leq 5 \leq 5 \leq 5	GRM32ER60J107M GRM32ER60J476M GRM32ER61C226K GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3 V 6.3 V 16 V 16 V	100 47 22 10	0.002 Ω		1210 case 3225mm	N/R ⁽²⁾ N/R ⁽²⁾ 1 ⁽⁴⁾ 1 ⁽⁴⁾	\leq 3 \leq 5 \leq 5 \leq 5	C3225X5R0J107MT C3225X5R0J476MT C3225X5R1C226MT C3225X5R1C106MT

(1) A total capacitance of 540 μ F is acceptable based on the combined ripple current rating.

(2) N/R – Not recommended. The capacitor voltage rating does not meet the minimum derated operating limits.

(3) The voltage rating of this capacitor only allows it to be used for output voltages that are equal to or less than 5.1 V.

(4) Ceramic capacitors may be used to compliment electrolytic types at the input to further reduce high-frequency ripple current.

Table 2 - Recommended Input/Output Capacitors

3. Mechanical Information

3.1 Mechanical Outline Drawings

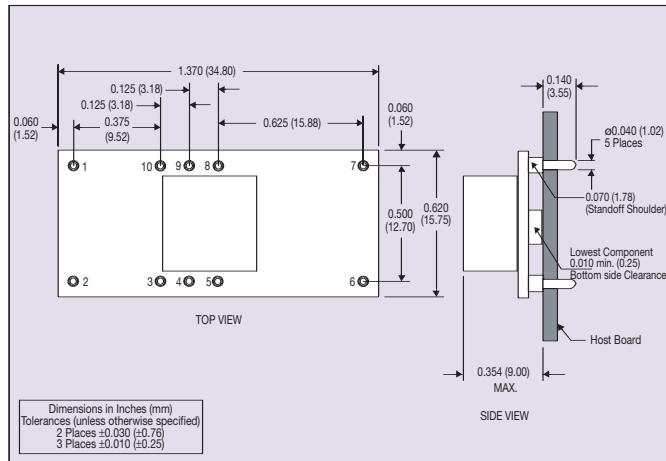


Figure 1 - Plated Through-Hole Mechanical Drawing

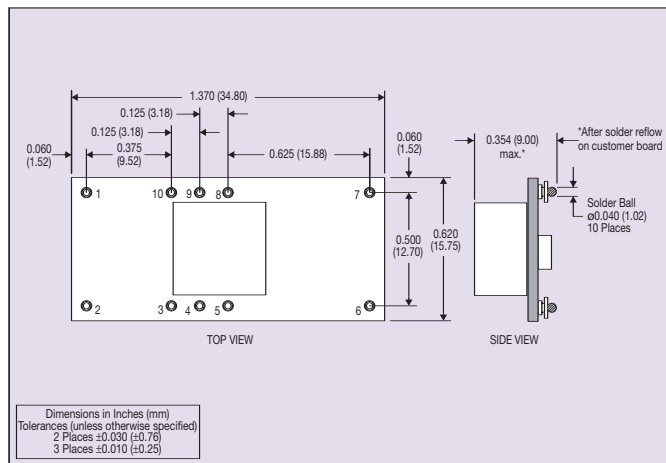


Figure 2 - Surface Mount Mechanical Drawing

3.2 Pin-out Table

PIN CONNECTIONS	
PIN NUMBER	FUNCTION
1	Ground
2	Vin
3	Inhibit
4	Vo Adjust
5	Vo Sense
6	Vout
7	Ground
8	Track
9	Margin Down
10	Margin Up

Table 3 - Pin Connections

3.3 Pin Description

3.3.1 Ground

This is the common ground connection for the Vin and Vout power connections. It is also the 0 Vdc reference for the control inputs.

3.3.2 Vin

The positive input voltage power node to the module, which is referenced to common GND.

3.3.3 Inhibit

The Inhibit pin is an open-collector/drain negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module will produce an output whenever a valid input source is applied.

3.3.4 Vo Adjust

A 1% resistor must be directly connected between this pin and pin 7 (GND) to set the output voltage to a value higher than its lowest value. The temperature stability of the resistor should be 100 ppm/°C or better. The set point range is from 1.2 V to 5.5 V for the 'W' suffix and 0.8 V to 1.8 V for the 'L' suffix. The resistor required for a given output voltage may be calculated from the equations in Section 7.1. If left open-circuit the output voltage will default to its lowest value. For further information on output voltage adjustment please see Section 7.1.

The specification table gives the preferred resistor values for a number of standard output voltages.

3.3.5 Vo Sense

The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy Vo Sense should be connected to Vout. It can also be left disconnected.

3.3.6 Vout

The regulated positive power output with respect to the GND node.

3.3.7 Track

This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the output will follow the voltage at the track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to Vin.

Note: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power-up. For more information, see Section 10.0.

3.3.8 Margin Down

When this input is asserted to GND, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is not TTL compatible. A lower percent change can be accommodated with a series resistor, see Section 7.3.

3.3.9 Margin Up

When this input is asserted to GND, the output voltage is increased by 5%. The input requires an open-collector (open-drain) interface. It is not TTL compatible. The percent change can be reduced with a series resistor, see Section 7.3.

4. Packaging Information

4.1 Packaging

The PTH12010 are available in trays of 20 units and tape and reel format in quantities of 250 units per reel.

Tray and tape dimensions including pick point are shown in the following diagrams.

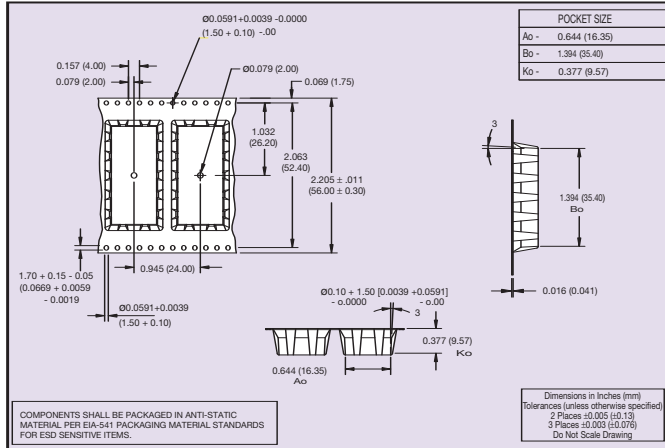


Figure 3 - Tape Dimensions

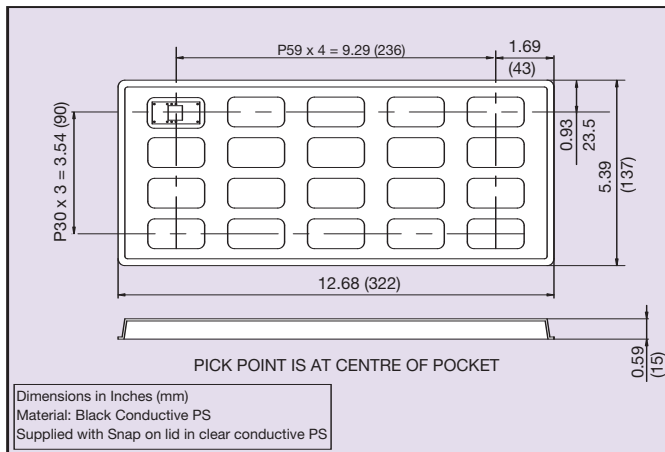


Figure 4 - Tray

4.2 Labelling and Part Numbering Sequence

All units in the series will be clearly marked to allow ease of identification for the end user. Figure 5 gives details of all the models

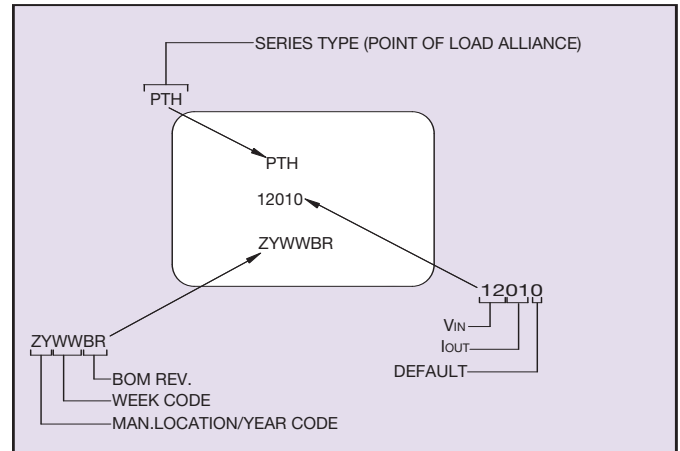


Figure 5 - PTH12010 Part Numbering

5. Safety Information

5.1 Safety Standards and Approvals

All models will have full international safety approval including EN60950 and UL/cUL1950. Models have been submitted to independent safety agencies for approval.

5.2 Fuse Information

Any suitable value fuse (based on the input ratings) maybe used in the unearthed input line. However this is not required for compliance with safety.

5.3 Safety Considerations

The converter must be installed as per guidelines outlined by the various safety agency approvals, if safety agency approval is required for the overall system.

6. Operating Information

6.1 Overtemperature Protection (OTP)

The PTHxx020 and PTHxx030 series of products have overtemperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold (see datasheet specifications), the module's Inhibit control is automatically pulled low. This disables the regulator allowing the output voltage to drop to zero. (The external output capacitors will be discharged by the load circuit). The recovery is automatic, and begins with a soft-start power-up. It occurs when the sensed temperature decreases by about 10 °C below the trip point.

Note: The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

6.2 Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold will cause the regulated output to shut down. Following shutdown a module will periodically attempt to recover by initiating a soft-start power-up. This is described as a "hiccup" mode of operation, whereby the module continues in the cycle of successive shutdown and power-up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

6.3 Soft-start Power-up

The Auto-Track™ feature allows the power-up of multiple PTH modules to be directly controlled from the Track pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage, V_{in} (see Figure 6).

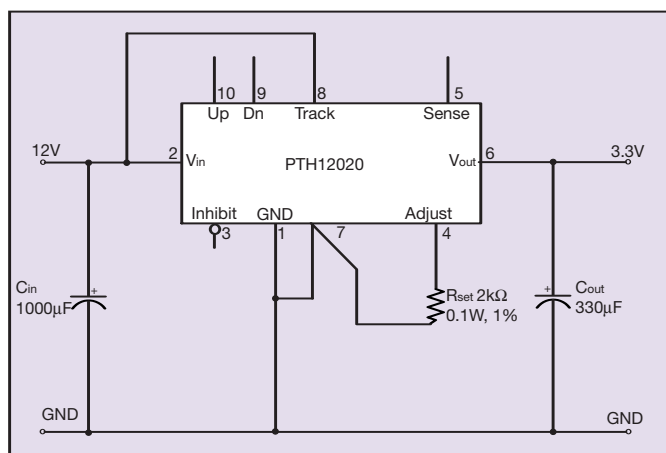
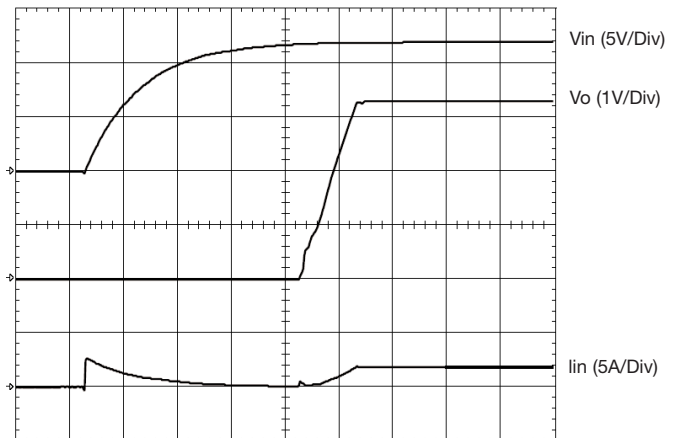


Figure 6 - Soft-start Power-up

When the Track pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power-up entirely under the control of its internal soft-start circuitry. When power-up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.



HORIZ SCALE: 5 ms/Div

Figure 7 - Power-up Characteristic

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 8 ms to 15 ms) before allowing the output voltage to rise. The output then progressively rises to the module's set-point voltage. Figure 7 shows the soft-start power-up characteristic of the 18 A output product (PTH12020W), operating from a 12 V input bus and configured for a 3.3 V output. The waveforms were measured with a 5 A resistive load, with Auto-Track disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 25 ms.

7. Feature Set

7.1 Adjusting the Output Voltage

The Vo adjust control (pin 4) sets the output voltage of the PTH12010 product. The adjustment range is from 1.2 V to 5.5 V for the Suffix 'W' model and 0.8 V to 1.8 V for the Suffix 'L' model. The adjustment method requires the addition of a single external resistor, Rset, that must be connected directly between the Vo Adjust and GND pins¹. Tables 4A and 4B give the preferred values for the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages the value of the required resistor can either be calculated using the following equations, or simply selected from the range of values given in Tables 5A and 5B. Figure 8 shows the placement of the required resistor.

$$R_{set} = 10K \times \frac{0.8V}{V_{out} - 1.2V} - 1.82 K\Omega$$

Equation 1 - 'W' Suffix Models

$$R_{set} = 10K \times \frac{0.8V}{V_{out} - 0.8V} - 7.87 K$$

Equation 2 - 'L' Suffix Models

V _{out} Standard	R _{set} (Pref'd Value)	V _{out} (Actual)
5.0 V	280 Ω	5.009 V
3.3 V	2.00 kΩ	3.294 V
2.5 V	4.32 kΩ	2.503 V
2.0 V	8.06 kΩ	2.010 V
1.8 V	11.50 kΩ	1.801 V
1.5 V	24.30 kΩ	1.506 V
1.2 V	Open	1.200 V

Table 4A - Preferred Values of R_{set} for Standard Output Voltages Suffix 'W' Models

V _{out} Standard	R _{set} (Pref'd Value)	V _{out} (Actual)
1.8 V	130 Ω	1.800 V
1.5 V	3.57 kΩ	1.499 V
1.2 V	12.1 kΩ	1.201 V
1.1 V	18.7 kΩ	1.101 V
1.0 V	32.4 kΩ	0.999 V
0.9 V	71.5 kΩ	0.901 V
0.8 V	Open	0.800 V

Table 4B - Preferred Values of R_{set} for Standard Output Voltages Suffix 'L' Models

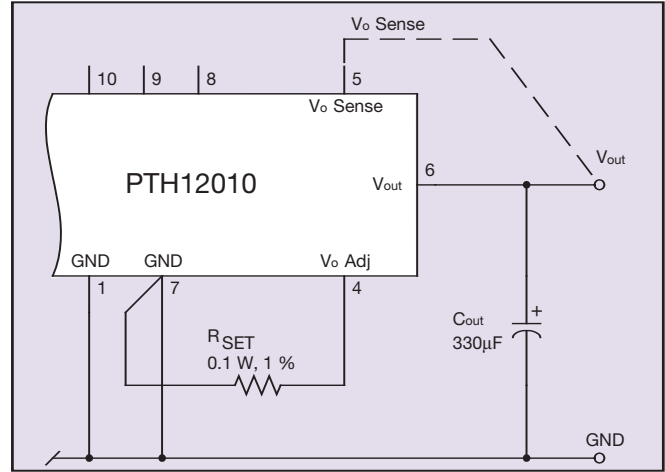


Figure 8 - Adjust Resistor Placement

OUTPUT VOLTAGE SET-POINT RESISTOR VALUES					
V _a Req'd	R _{set}	V _a Req'd	R _{set}	V _a Req'd	R _{set}
1.200	Open	2.15	6.6 kΩ	3.40	1.82 kΩ
1.225	318 kΩ	2.20	6.18 kΩ	3.45	1.74 kΩ
1.250	158 kΩ	2.25	5.8 kΩ	3.50	1.66 kΩ
1.275	105 kΩ	2.30	5.45 kΩ	3.55	1.58 kΩ
1.300	78.2 kΩ	2.35	5.14 kΩ	3.60	1.51 kΩ
1.325	62.2 kΩ	2.40	4.85 kΩ	3.70	1.38 kΩ
1.350	51.5 kΩ	2.45	4.85 kΩ	3.80	1.26 kΩ
1.375	43.9 kΩ	2.50	4.33 kΩ	3.90	1.14 kΩ
1.400	38.2 kΩ	2.55	4.11 kΩ	4.00	1.04 kΩ
1.425	33.7 kΩ	2.60	3.89 kΩ	4.10	939 Ω
1.450	30.2 kΩ	2.65	3.70 kΩ	4.20	847 Ω
1.475	27.3 kΩ	2.70	3.51 kΩ	4.30	761 Ω
1.50	24.8 kΩ	2.75	3.34 kΩ	4.40	680 Ω
1.55	21.0 kΩ	2.80	3.18 kΩ	4.50	604 Ω
1.60	18.2 kΩ	2.85	3.03 kΩ	4.60	533 Ω
1.65	16.0 kΩ	2.90	2.89 kΩ	4.70	466 Ω
1.70	14.2 kΩ	2.95	2.75 kΩ	4.80	402 Ω
1.75	12.7 kΩ	3.00	2.62 kΩ	4.90	342 Ω
1.80	11.5 kΩ	3.05	2.50 kΩ	5.00	285 Ω
1.85	10.5 kΩ	3.10	2.39 kΩ	5.10	231 Ω
1.90	9.61 kΩ	3.15	2.28 kΩ	5.20	180 Ω
1.95	8.85 kΩ	3.20	2.18 kΩ	5.30	131 Ω
2.00	8.18 kΩ	3.25	2.08 kΩ	5.40	85 Ω
2.05	7.59 kΩ	3.30	1.99 kΩ	5.50	41 Ω
2.10	7.07 kΩ	3.35	1.90 kΩ		

Table 5A - Output Voltage Set-point Resistor Values for Suffix 'W' Model

OUTPUT VOLTAGE SET-POINT RESISTOR VALUES					
V _a Req'd	R _{set}	V _a Req'd	R _{set}	V _a Req'd	R _{set}
0.800	Open	1.100	18.8 kΩ	1.400	5.46 kΩ
0.825	312 kΩ	1.125	16.7 kΩ	1.425	4.93 kΩ
0.850	152 kΩ	1.150	15 kΩ	1.450	4.44 kΩ
0.875	98.8 kΩ	1.175	13.5 kΩ	1.475	3.98 kΩ
0.900	72.1 kΩ	1.200	12.1 kΩ	1.500	3.56 kΩ
0.925	56.1 kΩ	1.225	11 kΩ	1.550	2.80 kΩ
0.950	45.5 kΩ	1.250	9.91 kΩ	1.600	2.13 kΩ
0.975	37.8 kΩ	1.275	8.97 kΩ	1.650	1.54 kΩ
1.000	32.1 kΩ	1.300	8.13 kΩ	1.700	1.02 kΩ
1.025	27.7 kΩ	1.325	7.37 kΩ	1.750	0.551 kΩ
1.050	24.1 kΩ	1.350	6.68 kΩ	1.800	0.130 kΩ
1.075	21.2 kΩ	1.375	6.04 kΩ		

Table 5B - Output Voltage Set-point Resistor Values for Suffix 'L' Model

Notes:

- Use a 0.1 W resistor, with a tolerance of 1% (or better). The tolerance should be 1%, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 7 using dedicated PCB traces.
- Never connect capacitors from Vo Adjust to either GND or Vout. Any capacitance added to the Vo Adjust pin will affect the stability of the regulator.

7.2 Output ON/OFF Inhibit

For applications requiring output voltage ON/OFF control, each series of the PTH family incorporates an output Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned OFF.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to Vin with respect to GND.

Figure 9 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit control has its own internal pull-up to +Vin potential. An open-collector or open-drain device is recommended to control this input. The input is not compatible with TTL logic devices.

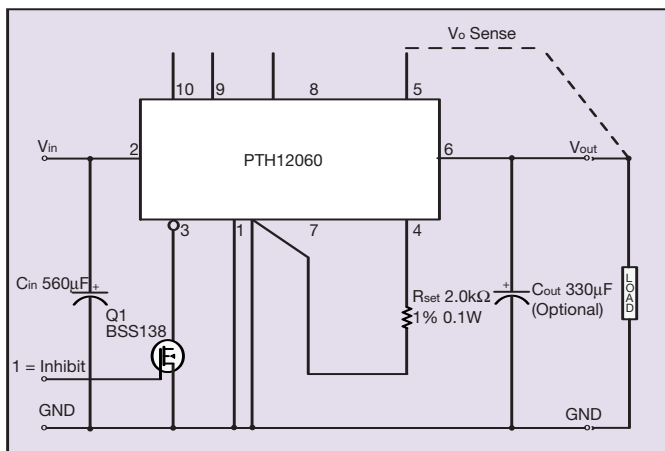


Figure 9 - Typical Application of the Inhibit Function

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module will execute a soft-start power-up sequence. A regulated output voltage is produced within 20 ms. Figure 10 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, Q1 Vds. The waveforms were measured with a 5 A load.

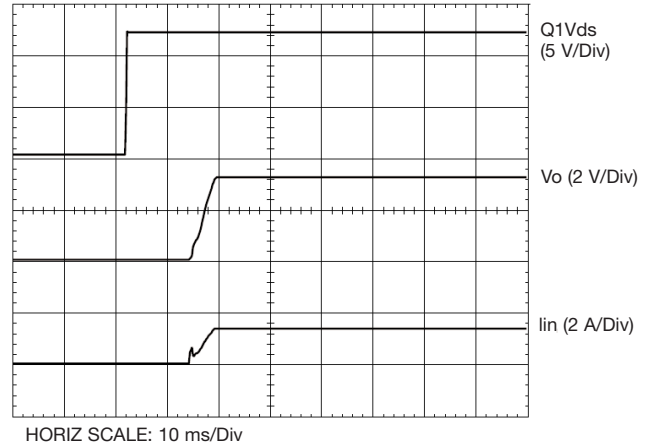


Figure 10 - Typical Rise in the Output Voltage and Input Current

7.3 Margin Up/Down Controls

The PTHxx060, PTHxx010, PTHxx020, and PTHxx030 module series incorporate Margin Up and Margin Down control inputs. These controls allow the output voltage set point to be momentarily adjusted¹, either up or down, by a nominal 5%. This provides a convenient method for dynamically testing the operation of the load circuit over its power supply margin or range. The ±5% change is applied to the adjusted output voltage as set by the external resistor, R_{Set} at the Vo Adjust pin.

The 5% adjustment is made by driving the appropriate margin control input directly to the GND terminal². A low-leakage open-drain device, such as a MOSFET or p-channel JFET is recommended for this purpose. Adjustments of less than 5% can also be accommodated by adding series resistors to the control inputs (see Figure 11). The value of the resistor can be selected from Table 6, or calculated using the following formula.

7.3.1 Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to something less than 5%, series resistors are required (See R_D and R_U in Figure 11). For the same amount of adjustment, the resistor value calculated for R_U and R_D will be the same. The equation is as follows:

$$R_U \text{ or } R_D = \frac{499}{\Delta\%} - 99.8 \quad \text{k}\Omega$$

Where Δ% = The desired amount of margin adjust in percent.

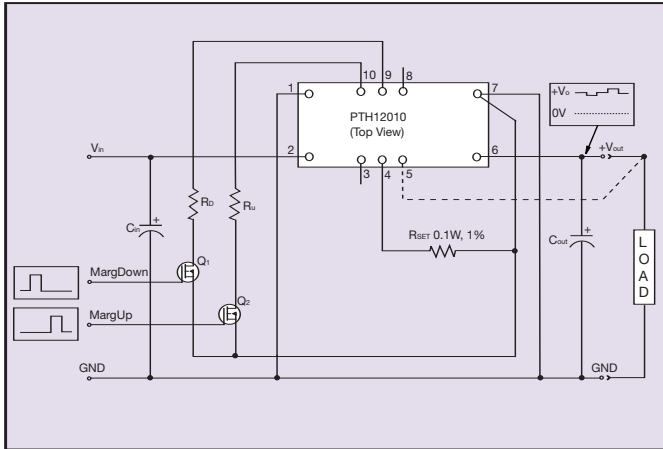


Figure 11 - Margin Up/Down Application Schematic

Notes:

- 1 The Margin Up and Margin Down controls were not intended to be activated simultaneously. If they are their effects on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
- 2 The ground reference should be a direct connection to the module GND at pin 7 (pin 1 for the PTHxx050). This will produce a more accurate adjustment at the load circuit terminals. The transistors Q1 and Q2 should be located close to the regulator.
- 3 The Margin Up and Margin Down control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 μ A when grounded, and has an open-circuit voltage of 0.8 V.

% ADJUST	R_U/R_D
1	397.0 k Ω
2	150.0 k Ω
3	66.5 k Ω
4	24.9 k Ω
5	0.0 k Ω

Table 6 - Margin Up/Down Resistor Values

7.4 Remote Sense

The V_o Sense pin should be connected to V_{out} at the load circuit (see datasheet standard application). A remote sense improves the load regulation performance of the module by allowing it to compensate for any 'IR' voltage drop between itself and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance. Use of the remote sense is optional. If not used, the V_o Sense pin can be left open-circuit. An internal low-value resistor (15 Ω or less) is connected between the V_o Sense and V_{out} , ensures that the output voltage remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_{out} and GND pins, and that measured from V_o Sense to GND, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components

that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

8. Thermal Information

8.1 Thermal Reference Points

The electrical operating conditions namely:

- Input voltage, V_{in}
- Output voltage, V_o
- Output current, I_o

determine how much power is dissipated within the converter. The following parameters further influence the thermal stresses experienced by the converter:

- Ambient temperature
- Air velocity
- Thermal efficiency of the end system application
- Parts mounted on system PCB that may block airflow
- Real airflow characteristics at the converter location

8.2 Safe Operating Area Curves

Thermal characterisation data is presented in the datasheet in a safe operating area curve format which is repeated here in Figures 12, 13 and 14. These SOA curves show the load current versus the ambient air temperature and velocity.

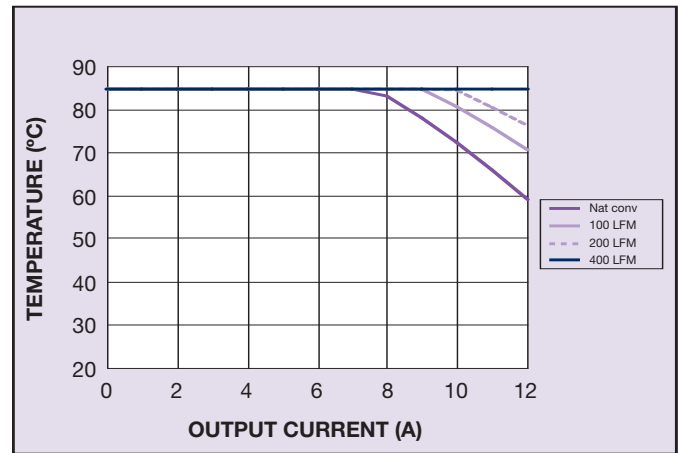


Figure 12 - Safe Operating Area
PTH12010 $V_{out} = 5$ V

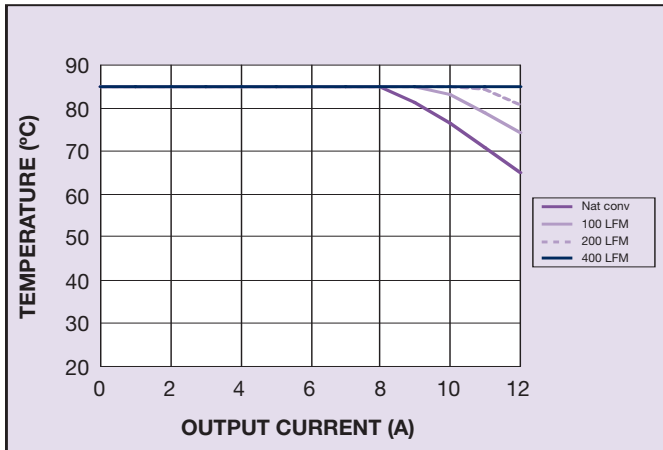


Figure 13 - Safe Safe Operating Area
PTH12010 $V_{out} = 3.3 V$

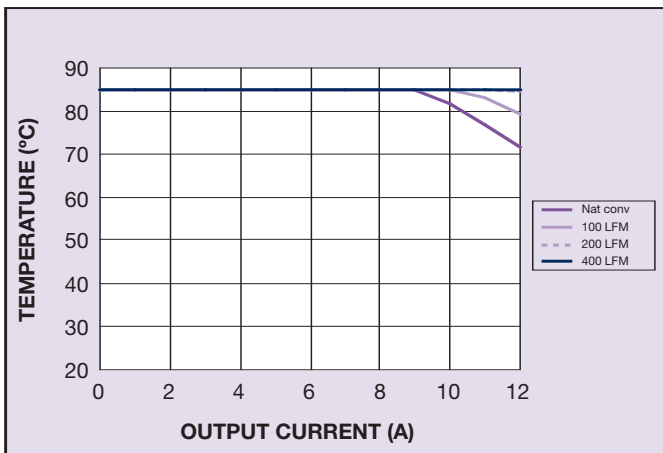


Figure 14 - Safe Operating Area
PTH12010 $V_{out} \leq 1.8 V$

8.3 Thermal Test Set-up

All of the data was taken with the converter soldered to a test board which closely represents a typical application. The test board is a 1.6 mm, eight layer FR4 PCB with the inner layers consisting of 2 oz power and ground planes. The top and bottom layers contain a minimal amount of metalization. A board to board spacing of 1 inch was used. The data represented by the 0 m/s curve indicate a natural convection condition i.e. no forced air. However, since the thermal performance is heavily dependent upon the final system application, the user needs to ensure the thermal reference point temperatures are kept within the recommended temperature rating. It is recommended that the thermal reference point temperatures are measured using either AWG #36 or #40 gauge thermocouples or an IR camera. In order to comply with stringent Artesyn derating criteria, the ambient temperature should never exceed 85 °C. Please contact Artesyn Technologies for further support.

9. Use in a Manufacturing Environment

9.1 Recommended Land Pattern

It is recommended that the customer uses a solder mask defined land pattern similar to that shown in the Figures 15 and 16:

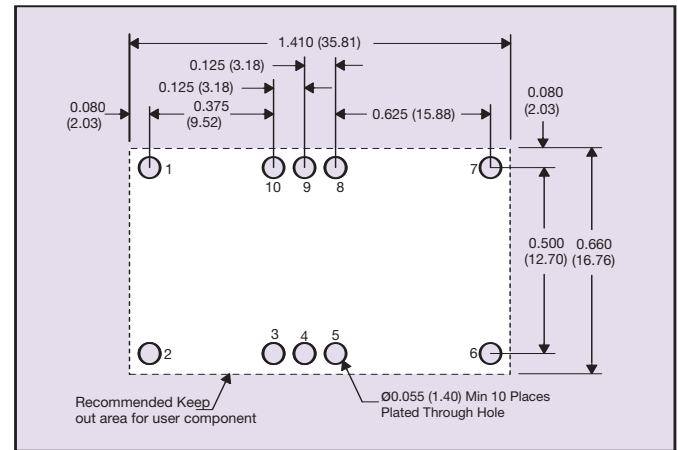


Figure 15 - Recommended Land Pattern (Through - Hole Model)

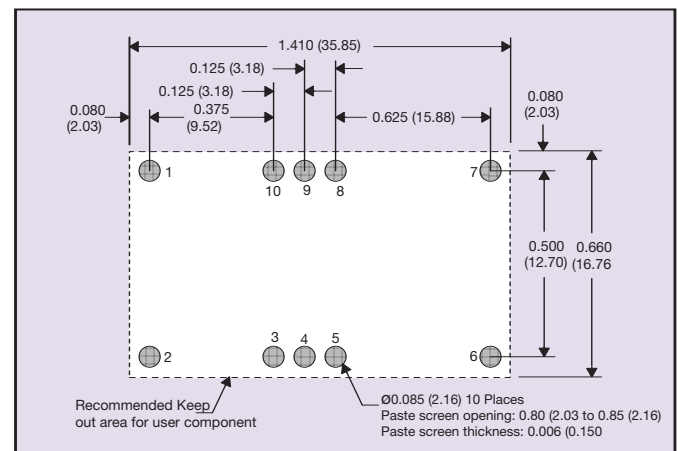


Figure 16 - Recommended Land Pattern (Surface Mount Model)

Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0.63) I.D. per input, ground and output pin (or the electrical equivalent).

As a surface-mount power component, interconnection to internal power planes will typically be required. This is accomplished by placing a number of vias between the SMT pad and the relevant plane. The number and exact location of these vias should be determined based on electrical resistivity, current flow and thermal requirements.

10. Auto-Track™

10.1 Auto-Track™ Function

The Auto-Track function is unique to the PTH family, and is available with the all “Point-of-Load Alliance” (POLA) products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power-up and power-down in sequence. The sequencing of two or more supply voltages during power-up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors, and ASICs.

10.2 How Auto-Track™ Works

Auto-Track works by forcing the module’s output voltage to follow a voltage presented at the Track control pin. This control range is limited to between 0 V and the module’s set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module’s output remains at its set-point¹. As an example, if the Track pin of a 2.5 V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

When under track control, the regulated output from the module follows the voltage at its Track pin on a volt for volt basis. By connecting the Track pin of a number of these modules together, the output voltages will follow a common signal during power-up and power-down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit³. The Track control also incorporates an internal RC charge circuit. This operates off the module’s input voltage to produce a suitable rising waveform at power-up.

10.3 Typical Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the Track control pins of two or more modules forces the Track control of all modules to follow the same collective RC ramp waveform, and allows them to be controlled through a single transistor or switch; Q1 in Figure 17.

To initiate a power-up sequence, it is recommended that the Track control be first pulled to ground potential. This should be done at or before input power is applied to the modules, and then held for at least 10 ms⁴ thereafter. This brief period gives the modules time to complete their internal soft-start initialization. Applying a logic level high signal to the circuit’s On/Off Control turns Q1 on and applies a ground signal to the Track pins. After completing their internal soft-start initialization, the output of all modules will remain at zero volts while Q1 is on.

10 ms after a valid input voltage has been applied to the modules, Q1 may be turned off. This allows the track control voltage to automatically rise toward to the modules’ input voltage. During this period the output voltage of each module will rise in unison with other modules, to its respective set-point voltage.

Figure 19 shows the output voltage waveforms from the circuit of Figure 18 after the ON/OFF Control is set from a high to a low-level voltage. The waveforms, V_{O1} and V_{O2} represent the output voltages from the two power modules, U1 (3.3 V) and U2 (2.0 V) respectively. V_{O1} and V_{O2} are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. Power-down is the reverse of power-up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power-down is complete. It also requires that Q1 be turned off relatively slowly. This is so that the Track control voltage does not fall faster than Auto-Track’s slew rate capability, which is 5 V/ms. The components R_1 and C_1 in Figure 17 limit the rate at which Q1 can pull down the Track control voltage. The values of 100 k Ω and 0.047 μ F correlate to a decay rate of about 0.6 V/ms.

The power-down sequence is initiated with a low-to-high transition at the ON/OFF Control input to the circuit. Figure 19 shows the power-down waveforms. As the Track control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track control.

Notes on the Use of Auto-Track™

1. The Track pin voltage must be allowed to rise above the module’s set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track function will track almost any voltage ramp during power-up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the Track pin is V_{in} . The open-circuit voltage is $0.56 \times V_{in}$, or 7.5 Vdc maximum.
4. The module will not follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the module has sensed that a valid voltage has been applied its input. During this period, it is recommended that the Track pin be held at ground potential.
5. The module is capable of both sinking and sourcing current when following a voltage at its Track pin. Therefore start-up into an output prebias cannot be supported when a module is under Auto-Track control.

Note: A pre-bias holdoff is not necessary when all supply voltages rise simultaneously under the control of Auto-Track.

6. The Auto-Track function can be disabled by connecting the Track pin to the input voltage (V_{in}). When Auto-Track is disabled, the output voltage will rise faster following the application of input power.

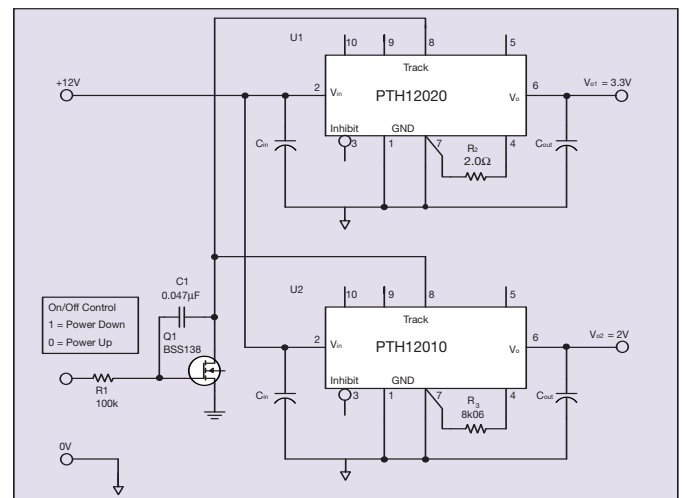


Figure 17 - Sequenced Power-up and Power-down Using Auto-Track™

11. Pre-Bias Start-up Capability

11.1 Pre-bias Start-up Capability

The capability to start-up into an output pre-bias condition is now available to all the 12 V input, PTH series of power modules. (Note that this is a feature enhancement for the many of the 'W' suffix products)⁽¹⁾. A pre-bias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes, sometimes used as part of a dual-supply power-up sequencing arrangement. A pre-bias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, such modules can sink as well as source output current. The 12 V input PTH modules all incorporate synchronous rectifiers, but will not sink current during start-up, or whenever the Inhibit pin is held low. Start-up includes an initial delay (approx. 8 ms to 15 ms), followed by the rise of the output voltage under the control of the module's internal soft-start mechanism; see Figure 20.

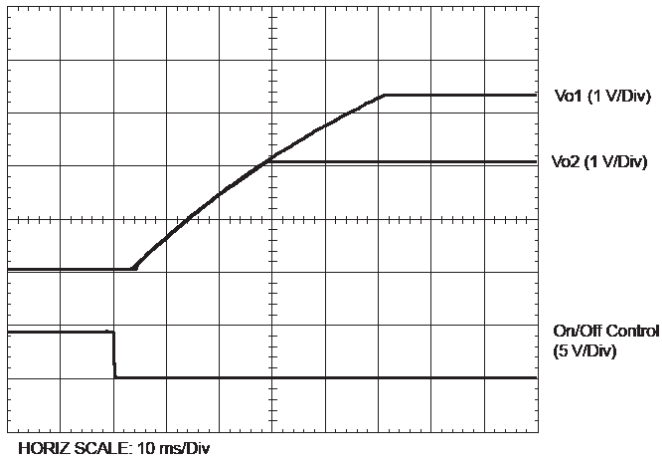


Figure 18 - Power-up with Auto-Track Control

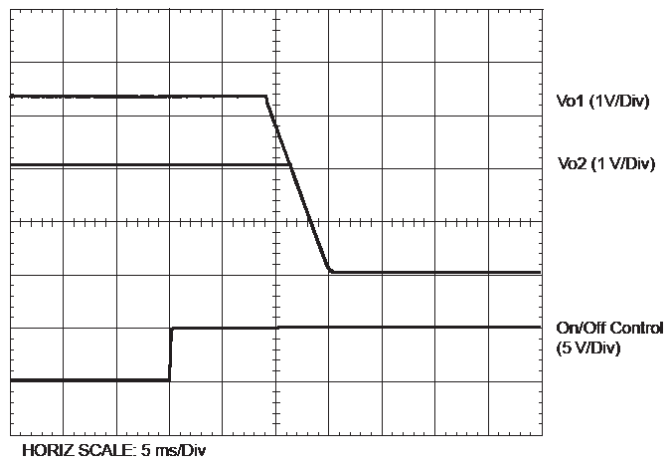


Figure 19 - Power-down with Auto-Track Control

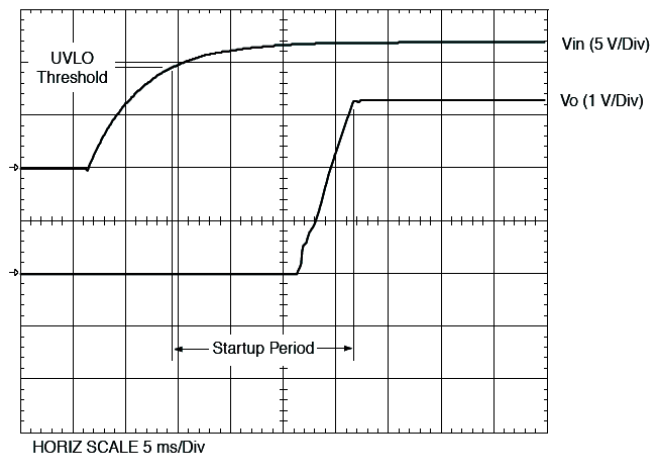


Figure 20 - PTH12020W Start-up

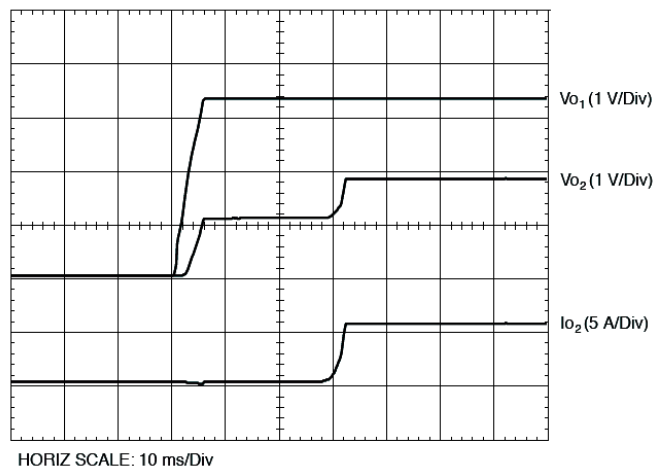


Figure 21 - Pre-Bias Start-up Waveforms

11.2 Conditions for Pre-Bias Holdoff

In order for the module to allow an output pre-bias voltage to exist (and not sink current), certain conditions must be maintained. The module holds off a pre-bias voltage when the Inhibit pin is held low, and whenever the output is allowed to rise under soft-start control. Power up under soft-start control occurs upon the removal of the ground signal to the Inhibit pin (with input voltage applied), or when input power is applied with Auto-Track disabled⁽²⁾. To further ensure that the regulator doesn't sink output current, (even with a ground signal applied to its Inhibit), the input voltage must always be greater than the applied pre-bias source. This condition must exist throughout the power-up sequence⁽³⁾.

The soft-start period is complete when the output begins rising above the pre-bias voltage. Once it is complete the module functions as normal, and will sink current if a voltage higher than the nominal regulation value is applied to its output.

Note: If a pre-bias condition is not present, the soft-start period will be complete when the output voltage has risen to either the set-point voltage, or the voltage applied at the module's Track control pin, whichever is lowest.

11.3 Demonstration Circuit

Figure 21 shows the startup waveforms for the demonstration circuit shown in Figure 22. The initial rise in Vo2 is the pre-bias voltage, which is passed from the VCCIO to the VCORE voltage rail through the ASIC. Note that the output current from the PTH12010L module (Io2) is negligible until its output voltage rises above the applied pre-bias.

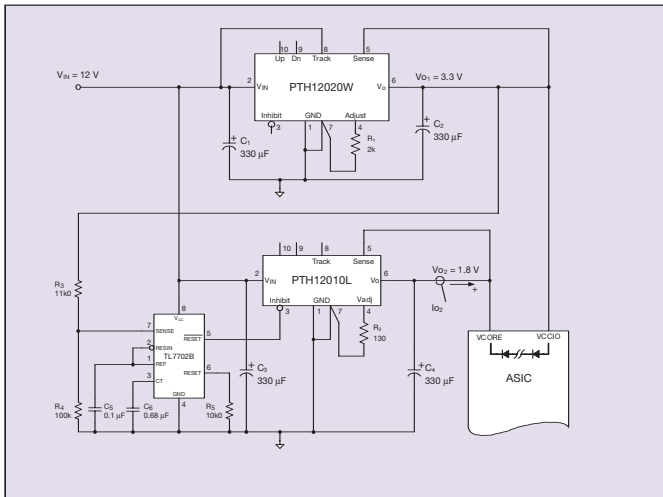


Figure 22 - Application Circuit Demonstrating Pre-Bias Start-up

Notes:

- 1 Output pre-bias holdoff is an inherent feature to all PTH120x0L and PTV120x0W/L modules. It has now been incorporated into all modules (including 'W' suffix modules with part numbers of the form PTH120x0W), with a production lot date code of '0530' or later.
- 2 The pre-bias start-up feature is not compatible with Auto-Track. If the rise in the output is limited by the voltage applied to the Track control pin, the output will sink current during the period that the track control voltage is below that of the back-feeding source. For this reason, it is recommended that Auto-Track be disabled when not being used. This is accomplished by connecting the Track pin to the input voltage, Vin. This raises the Track pin voltage well above the set-point voltage prior to the module's start up, thereby defeating the Auto-Track feature.
- 3 To further ensure that the regulator's output does not sink current when power is first applied (even with a ground signal applied to the Inhibit control pin), the input voltage must always be greater than the applied pre-bias source. This condition must exist throughout the power-up sequence of the power system.

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